LOW-NOISE LOW-DISTORTION GaAs FET AMPLIFIERS FOR 6 GHz SINGLE SIDEBAND RADIO

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ABSTRACT

This paper describes the design of a single-ended GaAs FET pre-amplifier using both computer aided device modeling and empirical methods. The amplifiers have an average noise figure of 2.3 dB, gain of 9 ± 0.5 dB, third-order distortion (M_{A+B-C}) of -50 dB and input-output return loss of 30 dB or more over the frequency band of 5.9 to 6.4 GHz.

Introduction

Microwave preamplifiers for single sideband and FM radio systems must meet stringent requirements[1] on gain, noise figure, distortion and return loss. GaAs FET single-ended amplifiers are designed using a combination of computer modeling (noise and distortion) and an empirical approach.

Modeling of GaAs FET

The device model parameters are obtained from the measured small signal S-parameters and the circuit topology of Figure 1 through computer optimization. S-parameter matching errors of less than a fraction of a dB in amplitude and less than 5° in phase are achieved. For noise behavior, in addition to the thermal noise sources associated with the parasitic resistances, two highly correlated noise sources, $\overline{i_{nd}^2}$ and $\overline{i_{ng}^2}$, are introduced.[2] Noise parameters for the short channel GaAs FET at the proper bias are extracted from noise measurements with several known terminations.

Third-order intermodulation is caused by the nonlinear nature of transconductance, g_m, and gate-source channel capacitance, Cgs. The nonlinear model is represented by the two nonlinear controlled current sources i_{Nd} and i_{Ng} replacing the two noise sources $\overline{i_{nd}^2}$ and and $\overline{i_{ng}^2}$ in Figure 1.

As a first order approximation, assuming unilateral condition (measured S_{12} <-25 dB), for a narrow-band, flat gain amplifier the third-order intermodulation index can be derived as

$$M_3 \approx \frac{20 \log \frac{3}{2} \left| \frac{j\omega C_3}{Y_1 (j\omega)} - \frac{g_3}{g_m} \right|}{|Z_{2T} (j\omega)|^2 \; |g_m|^2}$$

where ω is the intermodulation frequency component, $Y_1 (j\omega)$ is the admittance connected across i_{Ng} and $Z_{2T} (j\omega)$ is the transfer impedance from source i_{Nd} to the load. Coefficients g_3 and C_3 are related to the gate voltage V_g as

$$i_{Nd} = g_3 \, v_g^3$$

$$i_{Ng} = \frac{d}{dt} (C_3 \, v_g^3)$$

From extensive distortion measurements and as evidenced from the M_3 equation above, it is found that (1) g_m non-linearity is dominating and (2) M_3 is minimized for a maximum Z_{2T} i.e. output circuit designed for maximum gain.

Design Procedure

The design philosophy thus evolved is:

(a) Conjugately match the output for large gain. This should result in a design with near minimum non-linear distortion.

(b) Design the input network for good noise performance and

(c) Equalize the gain slope with the input network.

We have found that even small gain slope compensations at the output could degrade M_3 by as much as 6-8 dB, whereas at the input it results in a noise penalty of only about 0.1 - 0.15 dB.

A compromise bias point for low noise, low distortion and good gain is found to be around 1/2 of I_{dss}. An optimum noise source impedance is found using the noise model with constraints on noise figure, gain slope and input return loss given by design requirements. Input and output matching circuits are realized in microstrip configuration using a 25 mil ceramic substrate (ε_r = 10.2). To account for non-zero S_{12}, a couple of empirical interations will normally lead to optimal design.

Amplifier Performance

The MIC amplifier modules are soldered on a brass carrier. The biasing of the common source device from a -24V supply is

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achieved by d.c. floating the carrier. A passive fail-safe bypass[3] in suspended airline is also included so that in case of device or power supply failures, the amplifier will present no more than 10 dB (typically 7-8 dB) loss to the incoming signal. Waveguide to stripline transducers with return loss much greater than 30 dB form the input and output of the amplifier.

Packaged and sealed GaAs FET's were developed by Bell Laboratories, Murray Hill, New Jersey. The device alone has a noise figure of 1.4 - 1.6 dB. The performance of a typical amplifier including circulators and transducers is shown in Figures 2 to 5. The best achieved amplifier noise figure is under 2.0 dB. Temperature cycling the amplifiers from 40° to 120°F results in a maximum of 0.5 dB gain and 0.18 dB noise figure variation.

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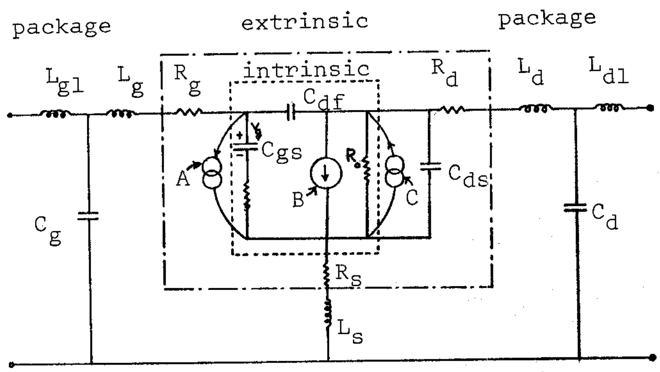
TABLE I

REQUIREMENTS[1]

Bandwidth:	5.925 - 6.425 GHz
Gain (dB):	$8 < G_o < 10$
Gain Flatness: (dB):	$G_o \pm 0.5$ over 500 MHz
Noise Figure:	≤ 3.0 dB
Linearity:	$M_{A+B-C} \leq -40$ dB
Unpowered Loss:	≤ 10 dB
Return Loss:	Input and Output ≥ 30 dB
RF Level:	-11 dBm Input
Environment:	40°F - 120°F with dry air (< 5% RH) in waveguide, 100% RH outside
DC Power:	-24 Volt office battery



B: $g_m v_g$, $g_m = g_{mo} \exp(-j\omega\tau)$,

FIGURE 1: EQUIVALENT CIRCUIT MODEL OF GAAS FET

A: $\overline{i_{ng}^2}$, C: $\overline{i_{nd}^2}$ for noise model

A: i_{Ng} , C: i_{Nd} for distortion model

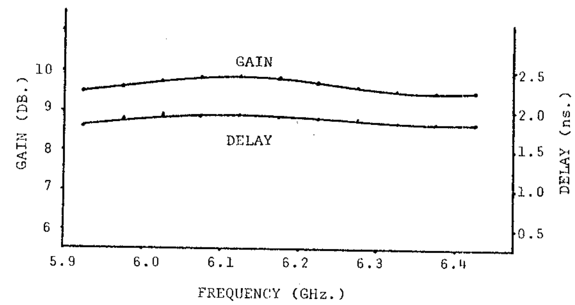


FIGURE 2: TYPICAL GAIN AND DELAY CHARACTERISTICS OF THE AMPLIFIER.

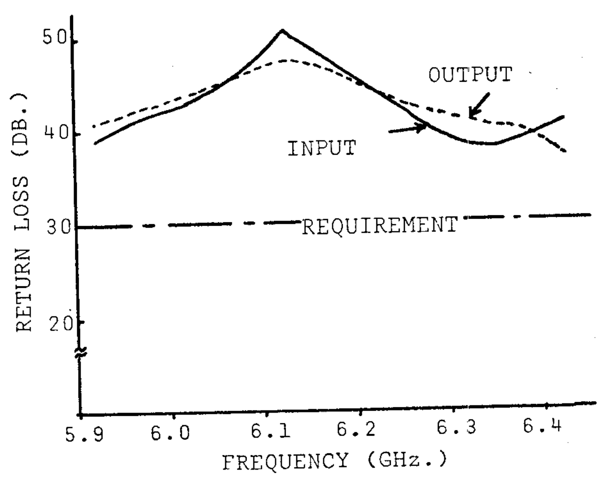


FIGURE 3: INPUT AND OUTPUT RETURN LOSS OF A TYPICAL AMPLIFIER

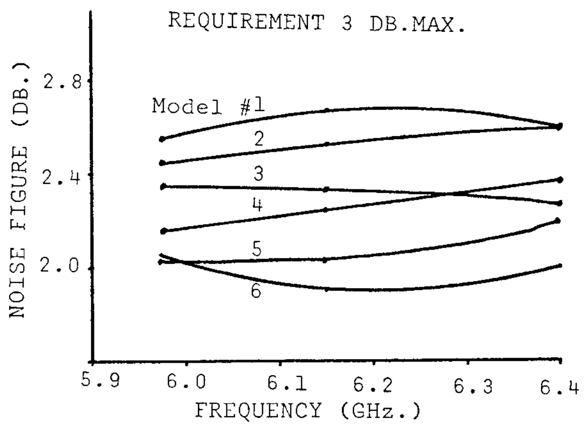


FIGURE 4: NOISE FIGURE VERSUS FREQUENCY BEHAVIOR OF THE AMPLIFIERS. AVERAGE NOISE FIGURE= 2.3DB.

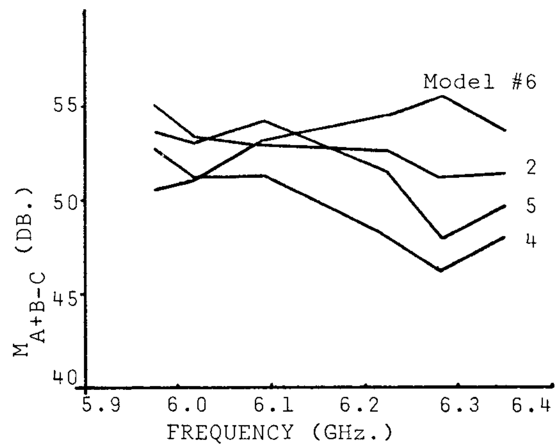


FIGURE 5: 3RD ORDER INTERMODULATION OF THE AMPLIFIERS MEASURED AT P out /TONE= -6.2 DBM. REQUIREMENT: -40 DB.